HEER HOME I SEARCH HEER I SHOP ! WEB ACCOUNT ! CONTACT HEER



	₩ <b>200 100</b>
	tions/Services Standards Conferences Careers/Jobs
	Welcome United States Patent and Trademark Office
	Peer Review Quick Links » Sc
O- Home O- What Can I Access? O- Log-out	Your search matched <b>71</b> of <b>1134355</b> documents.  A maximum of <b>500</b> results are displayed, <b>15</b> to a page, sorted by <b>Relevance Descending</b> order.
O Contents	Refine This Search:
O- Journals	You may refine your search by editing the current search expression or enterinew one in the text box.
* & Magazines	memory <near 5="">testing<and>(compare<near 10="">test)</near></and></near>
O- Conference Proceedings	Check to search within this result set
O- Standards	Results Key:
Search	JNL = Journal or Magazine CNF = Conference STD = Standard
O- By Author O- Basic O- Advanced O- GrossRef  C- Join IEEE	1 Board level reliability testing of μBGA <sup>(R)</sup> packaging with lead-free so attachment Solberg, V.; Electronics Packaging Technology Conference, 2000. (EPTC 2000). Proceeding 3rd, 5-7 Dec 2000 Pages:10 - 14
O- Establish IEEE	[Abstract] [PDF Full-Text (356 KB)] IEEE CNF
Web Account  Access the IEEE Member Digital Library	2 A transparent online memory test for simultaneous detection of functional faults and soft errors in memories  Thaller, K.; Steininger, A.;  Reliability, IEEE Transactions on , Volume: 52 , Issue: 4 , Dec. 2003  Pages:413 - 422
O- Access the REE Enterprise File Cabinet	[Abstract] [PDF Full-Text (421 KB)] IEEE JNL
E Frint Format	3 <b>Testing for coupled cells in random-access memories</b> Savir, J.; McAnney, W.H.; Vecchio, S.R.; Computers, IEEE Transactions on , Volume: 40 , Issue: 10 , Oct. 1991 Pages:1177 - 1180
	[Abstract] [PDF Full-Text (256 KR)] TEER IN

### 4 March U: a test for unlinked memory faults

van de Goer, A.J.; Gaydadjiev, G.N.;

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems], Volume: 144, Issue: 3, June 1997

Pages:155 - 160

#### [Abstract] [PDF Full-Text (640 KB)] IEE JNL

#### 5 March LR: a test for realistic linked faults

van de Goor, A.J.; Gaydadjiev, G.N.; Mikitjuk, V.G.; Yarmolik, V.N.; VLSI Test Symposium, 1996., Proceedings of 14th, 28 April-1 May 1996 Pages: 272 - 280

[Abstract] [PDF Full-Text (692 KB)] IEEE CNF

## 6 A parallel approach for testing multi-port static random access memories

Karimi, F.; Irrinki, S.; Crosbuy, T.; Lombardi, F.; Memory Technology, Design and Testing, IEEE International Workshop on, 20, 6-7 Aug. 2001 Pages:73 - 81

[Abstract] [PDF Full-Text (568 KB)] IEEE CNF

#### 7 A highly-efficient transparent online memory test

Thaller, K.;

Test Conference, 2001. Proceedings. International, 30 Oct.-1 Nov. 2001 Pages: 230 - 239

[Abstract] [PDF Full-Text (750 KB)] IEEE CNF

#### 8 BIST: required for embedded DRAM

Tanoi, S.;

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998 Pages:1149

[Abstract] [PDF Full-Text (84 KB)] IEEE CNF

# 9 Coupling fast Walsh transform with waveform relaxation technique analyze lossy coupled transmission lines

Songxin Qi; Quanrang Yang;

Microwave Symposium Digest, 1992., IEEE MTT-S International , 1-5 June 199 Pages: 897 - 899 vol.2

[Abstract] [PDF Full-Text (156 KB)] IEEE CNF

#### 10 Testing for coupled cells in random-access memories

Savir, J.; McAnney, W.H.; Vecchio, S.R.; Test Conference, 1989. Proceedings. 'Meeting the Tests of Time'., International, 29-31 Aug. 1989 Pages: 439 - 451

[Abstract] [PDF Full-Text (688 KB)] IEEE CNF

## 11 Test data compression and test time reduction using an embedded microprocessor

Sungbae Hwang; Abraham, J.A.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 11 , Issue: 5 , Oct. 2003 Pages:853 - 862

[PDF Full-Text (561 KB)] [Abstract]

## 12 Testing content-addressable memories using functional fault mode and march-like algorithms

Kun-Jin Lin; Cheng-Wen Wu;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions

on , Volume: 19 , Issue: 5 , May 2000

Pages: 577 - 588

[Abstract] [PDF Full-Text (296 KB)] **IEEE JNL** 

## 13 Detection of multiple transitions in delay fault test of SPARC64 microprocessor

Maruyama, D.; Kanuma, A.; Mochiyama, T.; Komatsu, H.; Sugiyama, Y.; Ito, Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conferer on, 7-11 Nov. 2004

Pages:893 - 898

[Abstract] [PDF Full-Text (706 KB)] **IEEE CNF** 

### 14 A reconfigurable digital IC tester implemented using the ARM Integrator rapid prototyping system

Fang Pang; Brandon, T.; Cockburn, B.; Hume, M.;

Electrical and Computer Engineering, 2004. Canadian Conference on , Volume

4, 2-5 May 2004

Pages:1931 - 1935 Vol.4

[Abstract] [PDF Full-Text (464 KB)]

## 15 Efficient seed utilization for reseeding based compression [logic testing]

Volkerink, E.H.; Mitra, S.;

VLSI Test Symposium, 2003. Proceedings. 21st, 27 April-1 May 2003

Pages: 232 - 237

[Abstract] [PDF Full-Text (280 KB)]

1 2 3 4 5 Next

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE - All rights reserved

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
11	2658	hsiao.in.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:36
L2	75	hsiao-k\$.in.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:37
L3	1	hsiao-k\$-t\$.in.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:37
L4	25090	test\$4 near3 memory	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:38
L5	18780	test\$4 near2 memory	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:38
L6	3983	(test\$4 near2 memory) same (microprocessor or CPU or computer or server or processor)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:40
L7	1036	(test\$4 near2 memory) and (signal near10 receiv\$4 near10 (microprocessor or CPU or computer or server or processor))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:41
L8	481	(test\$4 near2 memory) and ((clock\$1 adj2 signal\$1) near10 (microprocessor or CPU or computer or server or processor))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:43
L9	13855	((clock\$1 adj2 signal\$1) near10 (microprocessor or CPU or processor))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:44
L10	77	(((clock\$1 adj2 signal\$1) near10 (microprocessor or CPU or processor))) same compar\$5 same test\$3	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:45
L11	2	(((clock\$1 adj2 signal\$1) near10 (microprocessor or CPU or processor))) same compar\$5 same test\$3 same sort\$4	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:56
L12	2	(((test\$4 adj2 signal\$1) near10 (microprocessor or CPU or processor))) same compar\$5 same sort\$3	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:57
L13	5	(((test\$4 adj2 signal\$1) same (microprocessor or CPU or processor))) same compar\$5 same sort\$3	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 15:58

L14	0	(microprocessor near10 compar\$5 near10 sort\$3) same (test\$4 near2 (data or information or script\$1 or signal\$1))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:00
L15	6	(microprocessor same compar\$5 same sort\$3) same (test\$4 near2 (data or information or script\$1 or signal\$1))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:01
L16	147	compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:02
L17	34	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) and I4	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:02
L18	12	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) same I4	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:02
L19	1	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) and I4 and (714/718.ccls.)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:04
L20	4	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) and I4 and (365/201.ccls.)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:04
L21	0	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) and l4 and (324/765.ccls.)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:04
L22	0	(compar\$5 same sort\$3 same (test\$4 near2 (data or information or script\$1 or signal\$1))) and I4 and (324/763.ccls.)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/03/11 16:04